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EXAMINER	
MOORE, IAN N	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/646,833	TRAN ET AL.	
	Examiner	Art Unit	
	IAN N. MOORE	2463	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *06 October 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16 and 21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16,21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments, see page 5, filed 10/6/09, with respect to 35 U.S.C. 101 rejections of claims 1-16 and 21 have been fully considered and are persuasive. The 35 U.S.C. 101 rejections of claims 1-16 and 21 have been withdrawn.

2. Applicant's arguments with respect to claims 1-16 have been considered but are moot in view of the new ground(s) of rejection.

Regarding claims 1-16 and 21, the applicant argued that, "…applicants disagree that SDATA and SYNC lines alone are sufficient for communication serial multi-channel audio, because a clock line is also required in CrystalClear (hereinafter refers to CS4205), such that three lines are required in CS4205…Voth teaches that "each signal cable are at least two additional lines (see FIG. 2)...Voth describers at least two additional lines in referring to FIG. 2, appearing to require at least four lines total…Voth fails to teach that "only the first signal line and the second signal line from the 2-line...bus"...Voth fails to illustrate communication of multichannel audio….using only the data and clock line of Voth in CS4205 as the office action suggests, would appear to prevent transmission of serial multi-channel audio in CS4205, because the combination would lack a SYNC line, and therefore render CS4205 unsatisfactory for its intended purpose…propose modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification...Thus combination of CS4205 and Voth does not teach or suggest all of the distinguishing features…" in page 6-9.

In response to applicant's argument, the examiner respectfully disagrees with the argument above.

In response to argument, CS4205 disclose **a first signal line** (see FIG. on cover page; see FIG. 7, 14, 16-20, 35, includes SD data line (OUT, or SDOUT)) **and a second signal line** (see FIG. 7,14, SYNC/LRCLK line (SYNC & BIT_CLK; or SCLK & LRCLK); see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-5; page 54-58, paragraphs 6.3-9). Thus, it is clear that the SD data line and SYNC/LRCLK line are utilized to communication audio data successfully from controller to CODEC.

In response to argument on CS4205, the applicant arguments based on "whether there is two, three or more lines required or not required" is irrelevant since the claim does not recite "requiring anything". Thus, arguments based on un-claimed subject matter are irrelevant. If the applicant were referring "only" as "requirement", Voth clearly disclose such limitation in the combined system 35 U.S.C. 103 rejection as set forth below.

In response to argument on Voth, Voth discloses as follows:

Included in each single cable are at least two additional lines (see FIG. 2). The first additional line provides power from host device 102 that may be employed by pendant peripherals 104-106. The second additional line provides a common ground. By providing power to pendant peripherals 104-106, a pendant peripheral need not include its own power source, thereby enabling it to be lighter in weight, and smaller in size. (see col. 5, lines 60-65). (emphasis added)

In view of above, it is clear that Voth a single cable contains two additional lines by referring to FIG. 1. The rejection is based on FIG. 2, not FIG. 1. Nowhere in the above citation discloses that four lines were used in FIG. 2. Thus, applicant argument is clearly an error.

Voth discloses as follows: (see col. 6, lines 1-10) and FIG. 2.

FIG. 2 is a schematic diagram illustrating one embodiment of data and clock lines, and circuitry of pendant bus system 100 of FIG. 1, in accordance with the present invention. As seen **in FIG. 2, host-pendant peripheral system 200 includes host device 102 and pendant peripheral 104, coupled through clock$_1$ and a data$_1$ line.** Pendant peripheral 104 includes pendant controller 206, which is described in more detail in conjunction FIG. 3. (emphasis added)

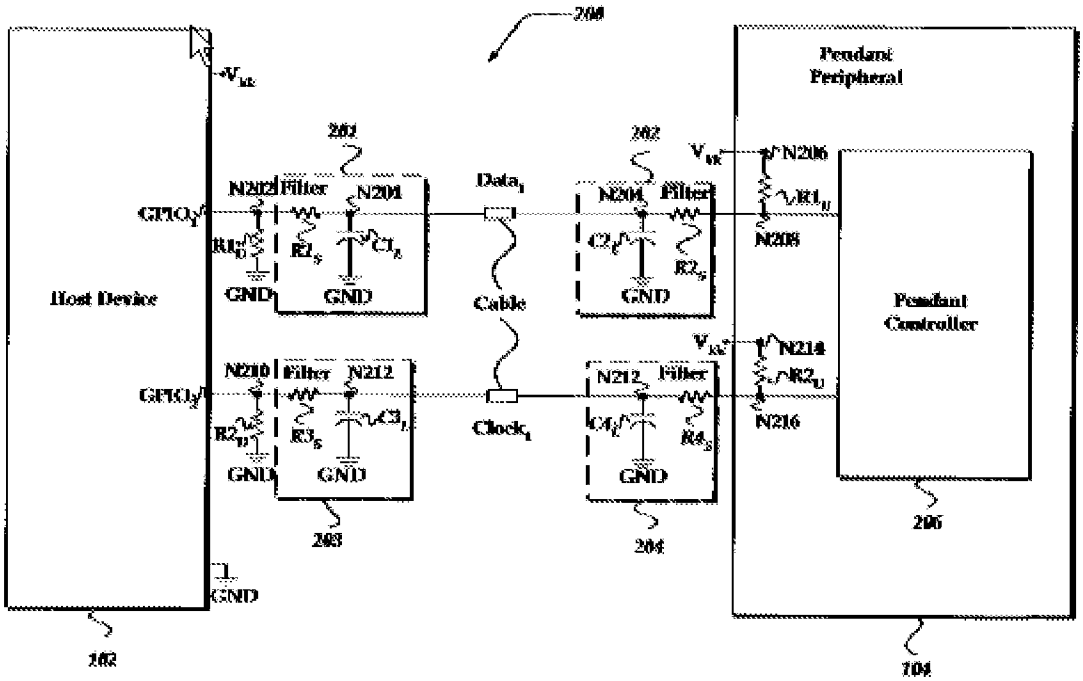

Fig. 2.

In view of above, it is clear that Voth discloses FIG. 2 uses clock$_1$ line and data$_1$ line. Thus, applicant argument that states that Voth FIG. 2 discloses four lines is clearly an error.

In response to applicant's arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In this case, the combined system of CS4205 and Voth clearly discloses the claimed invention.

CS4205 Reference discloses a method for communicating audio (see FIG. on cover page, FIG. 7, 16, Audio Codec (AC) communication system processing coding and decoding steps/methods), comprising: communication audio using a 2-line serial multi-channel audio interconnect data bus (**see FIG. on cover page; see FIG. 7, 14, 16-20, 35, communicating serial audio over multiple channels/lines interconnecting bus**) including only a first signal line (**see FIG. on cover page; see FIG. 7, 14, 16-20, 35, includes SD data line (OUT, or SDOUT)**) and a second signal line (**see FIG. 7,14, SYNC/LRCLK line (SYNC & BIT_CLK; or SCLK & LRCLK); see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-5; page 54-58, paragraphs 6.3-9**) wherein the first signal line (see FIG. on cover page; see FIG. 7, 14, SD data line (OUT, or SDOUT) and the second signal line are configured to communicate audio (see FIG. 7,14, and SYNC/LRCLK line (SYNC & BIT_CLK; or SCLK & LRCLK) are used to communicate audio PCM data ; see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-5; page 54-58, paragraphs 6.3-9; *note that per FIG. on cover page, FIG. 7, 14, SDATA_OUT signal line and SYNC signal line are sufficient/enough for communicating audio data; note that RESET # signal line is utilized for transmission of commands, and it is not required (i.e. optional) for communication audio data. Thus, it is clear that RESET signal is not required and thus it is not used for communication audio. SDATA_OUT signal line and SYNC signal line are used for communication audio; see page 13 section 2.1*; alternatively, per FIG. on cover page; per FIG. 7, 14, SDOUT signal line and LRCLK signal line are used for communicating audio data; *note that SCLK is optional in CS4205, and thus it is clear that SCLK signal is not required and thus it is not used for communication audio. SDATA_OUT signal line and LRCLK signal line are used for communication audio*; see page 53, section 6.1; see page 19-21, paragraphs

4,4.1,4.1.1-4.1.5; see page 54-56, paragraph 6.4,7) form the 2-line serial multi-channel audio interconnect data bus structured to communicate audio (see FIG. on cover page; see FIG. 7, 14; forming/configured as the serial audio over multiple channels/lines interconnecting bus to communicate/transmit/received audio data).

Voth teaches communication using a 2-line serial multi-channel interconnect data bus (FIG. 2, a 2-line host-pedant system using serial multi-lines/channel interconnect data bus system 200) including only a first signal line (FIG. 2, $data_1$ bus at $GPIO_1$) and a second signal line (FIG. 2, $clock_1$ bus at $GPIO_2$); abstract; see col. 6, line 1-50); wherein only the first signal line and the second signal line (FIG. 2, $data_1$ bus at $GPIO_1$ and $clock_1$ bus at $GPIO_2$) form the 2-line serial multi-channel interconnect data bus structured to communicate (FIG. 2, form/configure 2-line host-pedant system using serial multi-lines/channel interconnect data bus; see col. 6, line 1-50).

Thus, it is clear that the combined system of CS4205 and Voth clearly disclosed the claimed invention.

In response to applicant's argument that "therefore render CS4205 unsatisfactory for its intended purpose", the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981). In this case, examiner is not physically replacing "bodily incorporating" CS4205 system with Voth system. Rather, using the teaching of Voth to modify the CS4205. CS4205 uses a data line and a clock line, but fails to disclose "only" data line and clock line. Voth teaches the use of ONLY data line

and clock line. Thus, it is clear the combination of CS4205 and Voth would have been obvious to those of ordinary skill in the art by applying teaching of Voth into CS4205. Thus, there is no reason to provide unsatisfactory of its intended purpose.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, , it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide using "only" as taught by Voth in the system of CS4205, so that it would provide a general purpose, functional bus for chaining low-speed portable peripheral components; see Voth col. 1, line 40-60.

The previous responses to the argument on CS4205 are hereby incorporated.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-6, 8-16 and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over CS4205 (CyrstalClear Audio Codec '97 product information document) in view of Voth (US006957284B2) and Wolf (US007088398B1).

Regarding Claim 1, CS4205 Reference discloses a method for communicating audio (see FIG. on cover page, FIG. 7, 16, Audio Codec (AC) communication system processing coding and decoding steps/methods), comprising:

communication audio between a node (**see FIG. 7, between a digital AC node**) and decoder (**see FIG. 7, CODEC which include decoder**) using a 2-line serial multi-channel audio interconnects data bus (see FIG. on cover page; see FIG. 7, 14, 16-20, 35, communicating serial audio over multiple channels/lines interconnecting bus) including only a first signal line (see FIG. on cover page; see FIG. 7, 14, 16-20, 35, includes SD data line (OUT, or SDOUT)) and a second signal line (see FIG. 7,14, SYNC/LRCLK line (SYNC & BIT_CLK; or SCLK & LRCLK); see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-5; page 54-58, paragraphs 6.3-9);

transmitting, by the node, audio information segments on the first signal line (see FIG. transmission by a digital AC node on cover page; see FIG. 7, 14, 16-20, 35, SD data line (OUT, or SDOUT) transmits each audio frame segment/portion/frame), each segment (see FIG. 14, 17-20, each audio frame) including

(i) a format portion (see FIG. 14, 17-20, Slots 0-2) representative of audio format modes (see page 17-18, paragraph 3.2-3.4; pages 19-21, paragraphs 4, 4.1, 4.1.1-4.1.5; slots 0-2 contains audio format/arrangement/layout indication/signals (e.g. tags, command address,

command data) or modes (e.g. AC, Analog, digital, host processing, or multi-channel modes)) and

(ii) a data portion (see FIG. 14, 17-20, Slots 3-11) having audio data corresponding to one or more of the format modes (see page 17-18, paragraph 3.2-3.4; page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; see page 54-56, paragraph 6.4,7; slots 3-11 contains audio PCM data that corresponds/maps to the audio format/arrangement/layout indications/signals/modes); and

transmitting, by a node, a number of synchronization markers (see FIG. 7,14, transmitting by a digital AC node, SYNC pluses; see FIG. 17-20, transmitting LRCLK pulses) on the second signal line (see FIG. 7,14, SYNC/LRCLK line (SYNC & BIT_CLK; or SCLK & LRCLK); see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-5; page 54-58, paragraphs 6.3-9), each marker being representative of a timing of one of the audio information segments (see FIG. 14, 17-20; each SYNC/LRCLK pulse indicates the clock edge which defines a new serial data frame; see page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; see page 54-56, paragraph 6.4,7),

wherein the first signal line (see FIG. on cover page; see FIG. 7, 14, SD data line (OUT, or SDOUT) and the second signal line are configured to communicate audio (see FIG. 7,14, and SYNC/LRCLK line (SYNC & BIT_CLK; or SCLK & LRCLK) are used to communicate audio PCM data ; see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-5; page 54-58, paragraphs 6.3-9; *note that per FIG. on cover page, FIG. 7, 14, SDATA_OUT signal line and SYNC signal line are sufficient/enough for communicating audio data; note that RESET # signal line is utilized for transmission of commands, and it is not required (i.e. optional) for communication audio data. Thus, it is clear that RESET signal is not required and thus it is not used for communication audio. SDATA_OUT signal line and SYNC signal line are used for*

communication audio; see page 13 section 2.1; alternatively, per FIG. on cover page; per FIG. 7, 14, SDOUT signal line and LRCLK signal line are used for communicating audio data; *note that SCLK is optional in CS4205, and thus it is clear that SCLK signal is not required and thus it is not used for communication audio. SDATA_OUT signal line and LRCLK signal line are used for communication audio*; see page 53, section 6.1; see page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; see page 54-56, paragraph 6.4,7) form the 2-line serial multi-channel audio interconnect data bus structured to communicate audio (see FIG. on cover page; see FIG. 7, 14; forming/configured as the serial audio over multiple channels/lines interconnecting bus to communicate/transmit/received audio data).

Although CS4205 discloses using "a first signal line and a second signal line" as set forth above,

CS4205 does not explicitly disclose using "*only*" a first signal line and a second signal line.

However, Voth teaches communication using a 2-line serial multi-channel interconnect data bus (FIG. 2, a 2-line host-pedant system using serial multi-lines/channel interconnect data bus system 200) including only a first signal line (FIG. 2, $data_1$ bus at $GPIO_1$) and a second signal line (FIG. 2, $clock_1$ bus at $GPIO_2$); abstract; see col. 6, line 1-50);

wherein only the first signal line and the second signal line (FIG. 2, $data_1$ bus at $GPIO_1$ and $clock_1$ bus at $GPIO_2$) form the 2-line serial multi-channel interconnect data bus structured to communicate (FIG. 2, form/configure 2-line host-pedant system using serial multi-lines/channel interconnect data bus; see col. 6, line 1-50).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide using "only" as taught by Voth in the system of CS4205, so that it would provide a general purpose, functional bus for chaining low-speed portable peripheral components; see Voth col. 1, line 40-60.

Neither CS4205 nor Voth explicitly discloses "*encoder*".

However, Wolf discloses communicating audio between an encoder (see FIG. 1-2, TMDS transmitter 1 with encoder 2/4/6) and decoder (see FIG. 1-2, TMDS receiver 3 with decoder 8/10/12); and

transmitting by the encoder (see FIG. 1-2, transmitting by the encoder 2/4/6; see col. 11, line 30 to col. 13, line 26).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide "*encoder*" as taught by Wolf, in the combined system of CS4205 and Voth, so that it would provide transition minimized differential signaling which neither overlaps nor coincide with active encoded data; see Wolf col. 7, line 15-45.

Regarding Claim 2, CS4205 Reference discloses the audio comprises a serial bit stream (see page 13, paragraph 2.1; audio stream is a serial bit stream).

Regarding Claim 3, CS4205 Reference discloses the information segments are unmodulated (see page 17-18, paragraph 3.2-3.4; pages 19-24, paragraphs 4, 4.1, 4.1.1-4.1.5, 4.2-4.3; there is no modulation in CS4205, and thus it is clear that audio frames are no modulated in CS4205).

Regarding Claim 4, CS4205 Reference discloses the information segments are representative of one or more audio channels (see FIG. 14,17-20; see page 17-18, paragraph 3.2-

3.4; pages 19-24, paragraphs 4,4.1,4.1.1-4.1.5, 4.2-4.3;each audio frame represents one or more audio channels/slots).

Regarding Claim 5, CS4205 Reference discloses wherein the format portion comprises a total of 56 bit data word (see FIG. 14,17-20; see page 17-18, paragraph 3.2-3.4; page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; audio format/arrangement/layout indication/signals (e.g. tags, command address, command data) or modes (e.g. AC, Analog, digital, host processing, or multi-channel modes in slots 0-2 which contain total 56 bit data word).

Neither CS4205 nor Voth explicitly disclose "32 bits".

However, Wolf teaches the format portion comprises a 32 bit data word (see FIG. 9, 32 bits header; see col. 18, line 30-40; see col. 34, line 17-36).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide 32 bits header/format, as taught by Wolf in the combined system of CS4205 and Voth, so that it can transmit the header repeatedly over allowable clock period; see Wolf col. 18, line 34-41.

Regarding Claim 6, CS4205 Reference discloses wherein the format modes include at least one of an audio format (see page 17-18, paragraph 3.2-3.4; pages 19-21, paragraphs 4, 4.1, 4.1.1-4.1.5; audio format/arrangement/layout (e.g. audio tags/command address/ command data, or AC/Analog/digital/host processing/multi-channel mode)).

Regarding Claim 8, CS4205 Reference discloses the format modes are dynamic (see page 17-18, paragraph 3.2-3.4; pages 19-21, paragraphs 4,4.1,4.1.1-4.1.5; audio format/arrangement/layout (e.g. audio tags/command address/ command data, or

AC/Analog/digital/host processing/multi-channel mode) changes/varies from one frame to the other frame, thus the audio format/arrangement/layout are dynamic).

Regarding Claim 9, CS4205 Reference discloses the format modes are configured to vary from one information segment to another information segment (see page 17-18, paragraph 3.2-3.4; pages 19-21, paragraphs 4,4.1,4.1.1-4.1.5; audio format/arrangement/layout (e.g. audio tags/command address/ command data, or AC/Analog/digital/host processing/multi-channel mode) changes/varies from one frame to the other frame).

Regarding Claim 10, CS4205 Reference discloses the synchronization marker include sync pulses (see FIG. 14, 17-20; each SYNC/LRCLK pulse; see page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; see page 54-56, paragraph 6.4,7).

Regarding Claim 11, CS4205 Reference discloses each sync pulse represents a start of one information segment transmission (see FIG. 14, 17-20; each SYNC/LRCLK pulse indicates the clock edge which defines a new serial data frame; see page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; see page 54-56, paragraph 6.4,7).

Regarding Claim 12, CS4205 Reference discloses a method for communicating audio (see FIG. on cover page, FIG. 7, 16, Audio Codec (AC) communication system processing coding and decoding steps/methods), comprising:

communication audio between a node (**see FIG. 7, between a digital AC node**) and decoder (**see FIG. 7, CODEC which include decoder**) using a 2-line serial multi-channel audio interconnects data bus (see FIG. on cover page; see FIG. 7, 14, 16-20, 35, communicating serial audio over multiple channels/lines interconnecting bus) including only a first signal line (see FIG. on cover page; see FIG. 7, 14, 16-20, 35, includes SD data line (IN&OUT, or SDOUT &

SDI1-3)) and a second signal line (see FIG. 7,14, SYNC/LRCLK line (SYNC & BIT_CLK; or SCLK & LRCLK); see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-5; page 54-58, paragraphs 6.3-9);

receiving, by the decoder, audio information segments on the first signal line (see FIG. on cover page; see FIG. 7, 14, 16-20, 35, receiving at CODEC which include decoder SD data line (IN&OUT, or SDOUT & SDI1-3), each segment including

(i) a format portion (see FIG. 14, 17-20, Slots 0-2) representative of audio format modes (see page 17-18, paragraph 3.2-3.4; pages 19-24, paragraphs 4,4.1,4.1.1-4.1.5, 4.2-4.3; slots 0-2 contains audio format/arrangement/layout indication/signals (e.g. tags, command address, command data) or modes (e.g. AC, Analog, digital, host processing, or multi-channel modes)) and

(ii) a data portion (see FIG. 14, 17-20, Slots 3-11) having audio data corresponding to one or more of the format modes (see page 17-18, paragraph 3.2-3.4; pages 19-24, paragraphs 4,4.1,4.1.1-4.1.5, 4.2-4.3; see page 54-56, paragraph 6.4,7; slots 3-11 contains audio PCM data that corresponds/maps to the audio format/arrangement/layout indications/signals/modes); and

receiving by the decoder a number of synchronization markers (see FIG. 14, receiving SYNC pluses at CODEC which include decoder; see FIG. 17-20, transmitting LRCLK pulses) on the second signal line (see FIG. 7,14, SYNC/LRCLK line (SYNC & BIT_CLK; or SCLK & LRCLK); see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-5; page 54-58, paragraphs 6.3-9), each marker being represented of a timing of one of the audio segments (see FIG. 14, 17-20; each SYNC/LRCLK pulse indicates the clock edge which defines a new serial data frame; see page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; see page 54-56, paragraph 6.4,7),

wherein the first signal line (see FIG. on cover page; see FIG. 7, 14, SD data line (OUT, or SDOUT) and the second signal line (see FIG. 7,14, SYNC/LRCLK line (SYNC & BIT_CLK; or SCLK & LRCLK); see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-5; page 54-58, paragraphs 6.3-9) are used to communicate audio (see FIG. 7,14, and SYNC/LRCLK line (SYNC & BIT_CLK; or SCLK & LRCLK) are arranged/configured to communicate audio PCM data ; see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-5; page 54-58, paragraphs 6.3-9); *note that per FIG. on cover page, FIG. 7, 14, SDATA_OUT signal line and SYNC signal line are sufficient/enough for communicating audio data; note that RESET # signal line is utilized for transmission of commands, and it is not required (i.e. optional) for communication audio data. Thus, it is clear that RESET signal is not required and thus it is not used for communication audio. SDATA_OUT signal line and SYNC signal line are used for communication audio; see page 13 section 2.1*; Alternatively, per FIG. on cover page; per FIG. 7, 14, SDOUT signal line and LRCLK signal line are used for communicating audio data; *note that SCLK is optional in CS4205, and thus it is clear that SCLK signal is not required and thus it is not used for communication audio. Only SDATA_OUT signal line and LRCLK signal line are used for communication audio*; see page 53, section 6.1; see page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; see page 54-56, paragraph 6.4,7) form the 2-line serial multi-channel audio interconnect data bus structured to communicate audio (see FIG. on cover page; see FIG. 7, 14; forming/configured as the serial audio over multiple channels/lines interconnecting bus to communicate/transmit/received audio data).

Although CS4205 discloses using "a first signal line and a second signal line" as set forth above,

CS4205 does not explicitly disclose using "*only*" a first signal line and a second signal line.

However, Voth teaches communication using a 2-line serial multi-channel interconnect data bus (FIG. 2, a 2-line host-pedant system using serial multi-lines/channel interconnect data bus system 200) including only a first signal line (FIG. 2, $data_1$ bus at $GPIO_1$) and a second signal line (FIG. 2, $clock_1$ bus at $GPIO_2$); abstract; see col. 6, line 1-50); .

wherein only the first signal line and the second signal line (FIG. 2, $data_1$ bus at $GPIO_1$ and $clock_1$ bus at $GPIO_2$) form the 2-line serial multi-channel interconnect data bus structured to communicate (FIG. 2, form/configure 2-line host-pedant system using serial multi-lines/channel interconnect data bus; see col. 6, line 1-50).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide using "only" as taught by Voth in the system of CS4205, so that it would provide a general purpose, functional bus for chaining low-speed portable peripheral components; see Voth col. 1, line 40-60.

Neither CS4205 nor Voth explicitly discloses "*encoder*".

However, Wolf discloses communicating audio between an encoder (see FIG. 1-2, TMDS transmitter 1 with encoder 2/4/6) and decoder (see FIG. 1-2, TMDS receiver 3 with decoder 8/10/12; see col. 11, line 30 to col. 13, line 26).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide "*encoder*" as taught by Wolf, in the combined system of CS4205 and Voth, so that it would provide transition minimized differential signaling which neither overlaps or coincide with active encoded data; see Wolf col. 7, line 15-45.

Regarding Claim 13, CS4205 Reference discloses the information segments are unmodulated (see page 17-18, paragraph 3.2-3.4; pages 19-24, paragraphs 4, 4.1, 4.1.1-4.1.5, 4.2-4.3; there is no modulation in CS4205, and thus it is clear that audio frames are no modulated in CS4205).

Regarding Claim 14, CS4205 Reference discloses the information segments are representative of one or more audio channels (see FIG. 14,17-20; see page 17-18, paragraph 3.2-3.4; pages 19-24, paragraphs 4,4.1,4.1.1-4.1.5, 4.2-4.3;each audio frame represents one or more audio channels/slots).

Regarding Claim 15, CS4205 Reference discloses wherein the format portion comprises a total of 56 bit data word (see FIG. 14,17-20; see page 17-18, paragraph 3.2-3.4; page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; audio format/arrangement/layout indication/signals (e.g. tags, command address, command data) or modes (e.g. AC, Analog, digital, host processing, or multi-channel modes in slots 0-2 which contain total 56 bit data word).

Neither CS4205 nor Voth explicitly disclose 32 bits.

However, Wolf teaches the format portion comprises a 32 bit data word (see FIG. 9, 32 bits header; see col. 18, line 30-40; see col. 34, line 17-36).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide 32 bits header/format, as taught by Wolf in the combined system of CS4205 and Voth, so that it can transmit the header repeatedly over allowable clock period; see Wolf col. 18, line 34-41.

Regarding Claim 16, CS4205 Reference discloses each sync pulse represents a start of one information segment transmission (see FIG. 14, 17-20; each SYNC/LRCLK pulse indicates

the clock edge which defines a new serial data frame; see page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; see page 54-56, paragraph 6.4,7).

Regarding Claim 21, CS4205 Reference discloses a system for communicating audio (see FIG. on cover page, FIG. 7, 16, Audio Codec (AC) communication system processing coding and decoding steps/methods), comprising:

a 2-line serial multi-channel audio interconnect data bus configured to communicate audio (see FIG. on cover page; see FIG. 7, 14, 16-20, 35, communicating serial audio over multiple channels/lines interconnecting bus), including only a first signal line (see FIG. on cover page; see FIG. 7, 14, 16-20, 35, includes SD data line (OUT, or SDOUT)) and a second signal line (see FIG. 7,14, SYNC/LRCLK line (SYNC & BIT_CLK; or SCLK & LRCLK); see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-5; page 54-58, paragraphs 6.3-9);

a node (**see FIG. 7, between a digital AC node**) coupled to the 2-line serial multi-channel audio interconnect data bus (see FIG. on cover page; see FIG. 7, 14, 16-20, 35, connects to serial audio over multiple channels/lines interconnecting bus), and configured to transmit audio information segments on the first signal line (see FIG. transmission by a digital AC node on cover page; see FIG. 7, 14, 16-20, 35, SD data line (OUT, or SDOUT) transmits each audio frame segment/portion/frame), each segment segment (see FIG. 14, 17-20, each audio frame) including

(i) a format portion (see FIG. 14, 17-20, Slots 0-2) representative of audio format modes (see page 17-18, paragraph 3.2-3.4; pages 19-21, paragraphs 4, 4.1, 4.1.1-4.1.5; slots 0-2 contains audio format/arrangement/layout indication/signals (e.g. tags, command address,

command data) or modes (e.g. AC, Analog, digital, host processing, or multi-channel modes)) and

(ii) a data portion (see FIG. 14, 17-20, Slots 3-11) having audio data corresponding to one or more of the format modes (see page 17-18, paragraph 3.2-3.4; page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; see page 54-56, paragraph 6.4,7; slots 3-11 contains audio PCM data that corresponds/maps to the audio format/arrangement/layout indications/signals/modes); and

the node further configured to transmit a number of synchronization markers (see FIG. 7,14, transmitting by a digital AC node, SYNC pluses; see FIG. 17-20, transmitting LRCLK pulses) on the second signal line (see FIG. 7,14, SYNC/LRCLK line (SYNC & BIT_CLK; or SCLK & LRCLK); see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-5; page 54-58, paragraphs 6.3-9), each marker being representative of a timing of one of the audio information segments (see FIG. 14, 17-20; each SYNC/LRCLK pulse indicates the clock edge which defines a new serial data frame; see page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; see page 54-56, paragraph 6.4,7),

a decoder (see FIG. 7, CODEC which include decoder) coupled to the 2-line serial multi-channel audio interconnect data bus (see FIG. on cover page; see FIG. 7, 14, 16-20, 35, connects with serial audio over multiple channels/lines interconnecting bus) and configured to receive the audio information segments on the first signal line (see FIG. on cover page; see FIG. 7, 14, 16-20, 35, receiving at CODEC which include decoder SD data line (IN&OUT, or SDOUT & SDI1-3), the decoder further configured to receive a number of the synchronization markers (see FIG. 14, receiving SYNC pluses at CODEC which include decoder; see FIG. 17-20, transmitting LRCLK pulses) on the second signal line (see FIG. 7,14, SYNC/LRCLK line (SYNC &

BIT_CLK; or SCLK & LRCLK); see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-5; page 54-58, paragraphs 6.3-9),

receiving by the decoder a number of synchronization markers (see FIG. 14, receiving SYNC pluses at CODEC which include decoder; see FIG. 17-20, transmitting LRCLK pulses) on the second signal line (see FIG. 7,14, SYNC/LRCLK line (SYNC & BIT_CLK; or SCLK & LRCLK); see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-5; page 54-58, paragraphs 6.3-9), each marker being represented of a timing of one of the audio segments (see FIG. 14, 17-20; each SYNC/LRCLK pulse indicates the clock edge which defines a new serial data frame; see page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; see page 54-56, paragraph 6.4,7),

wherein the first signal line (see FIG. on cover page; see FIG. 7, 14, SD data line (OUT, or SDOUT) and the second signal line (see FIG. 7,14, SYNC/LRCLK line (SYNC & BIT_CLK; or SCLK & LRCLK); see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-5; page 54-58, paragraphs 6.3-9) are used to communicate audio (see FIG. 7,14, and SYNC/LRCLK line (SYNC & BIT_CLK; or SCLK & LRCLK) are arranged/configured to communicate audio PCM data ; see page 13-14, paragraph 2.1,2.2; page 19-24, paragraphs 4-5; page 54-58, paragraphs 6.3-9); *note that per FIG. on cover page, FIG. 7, 14, SDATA_OUT signal line and SYNC signal line are sufficient/enough for communicating audio data; note that RESET # signal line is utilized for transmission of commands, and it is not required (i.e. optional) for communication audio data. Thus, it is clear that RESET signal is not required and thus it is not used for communication audio. SDATA_OUT signal line and SYNC signal line are used for communication audio; see page 13 section 2.1*; Alternatively, per FIG. on cover page; per FIG. 7, 14, SDOUT signal line and LRCLK signal line are used for communicating audio data; *note*

that SCLK is optional in CS4205, and thus it is clear that SCLK signal is not required and thus it is not used for communication audio. Only SDATA_OUT signal line and LRCLK signal line are used for communication audio; see page 53, section 6.1; see page 19-21, paragraphs 4,4.1,4.1.1-4.1.5; see page 54-56, paragraph 6.4,7) form the 2-line serial multi-channel audio interconnect data bus structured to communicate audio (see FIG. on cover page; see FIG. 7, 14; forming/configured as the serial audio over multiple channels/lines interconnecting bus to communicate/transmit/received audio data).

Although CS4205 discloses using "a first signal line and a second signal line" as set forth above,

CS4205 does not explicitly disclose using "*only*" a first signal line and a second signal line.

However, Voth teaches communication using a 2-line serial multi-channel interconnect data bus (FIG. 2, a 2-line host-pedant system using serial multi-lines/channel interconnect data bus system 200) including only a first signal line (FIG. 2, $data_1$ bus at $GPIO_1$) and a second signal line (FIG. 2, $clock_1$ bus at $GPIO_2$); abstract; see col. 6, line 1-50); .

wherein only the first signal line and the second signal line (FIG. 2, $data_1$ bus at $GPIO_1$ and $clock_1$ bus at $GPIO_2$) form the 2-line serial multi-channel interconnect data bus structured to communicate (FIG. 2, form/configure 2-line host-pedant system using serial multi-lines/channel interconnect data bus; see col. 6, line 1-50).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide using "only" as taught by Voth in the system of CS4205, so

that it would provide a general purpose, functional bus for chaining low-speed portable peripheral components; see Voth col. 1, line 40-60.

Neither CS4205 nor Voth explicitly discloses "*encoder*".

However, Wolf discloses communicating audio between an encoder (see FIG. 1-2, TMDS transmitter 1 with encoder 2/4/6) and decoder (see FIG. 1-2, TMDS receiver 3 with decoder 8/10/12; see col. 11, line 30 to col. 13, line 26).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide "*encoder*" as taught by Wolf, in the combined system of CS4205 and Voth, so that it would provide transition minimized differential signaling which neither overlaps nor coincide with active encoded data; see Wolf col. 7, line 15-45.

5. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over CS4205 in view of Voth and Wolf, and further in view of Wakazu (US006006287A).

Regarding Claim 7, CS4205 Reference discloses wherein the format modes include at least one of an audio format (see page 17-18, paragraph 3.2-3.4; pages 19-21, paragraphs 4,4.1,4.1.1-4.1.5; slots 0-2 contains audio format/arrangement/layout (e.g. audio tags/command address/ command data, or AC/Analog/digital/host processing/multi-channel mode)), and transmission of one or more one or more of the transmitted audio segments/frames to an intended recipient (see FIG. 7, controller, see FIG. 16, Stereo DACs) as set forth above in claim 1.

Neither CS4205, Voth nor Wolf explicitly discloses audio stream ID includes an indication of an intended recipient.

However, Wakazu teaches the audio stream ID (see FIG. 4, Audio stream ID 2; see FIG. 6, Audio stream IDs A1-A5) includes an indication of an intended recipient of one or more of the transmitted audio segments (see FIG. 2, audio stream ID indicates/identifies the receiver processor 211 or processor 210; see col. 5, line 10 to col. 6, line 60).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to provide audio stream ID includes an indication of an intended recipient, as taught by Wakazu in the combined system of CS4205, Voth and Wolf, so that it can separate/detect the received data stream according to the stream ID; see Wakazu col. 2, line 10-15, 40-49.

Conclusion

6. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to IAN N. MOORE whose telephone number is (571)272-3085. The examiner can normally be reached on 7:30 AM- 4:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Derrick W. Ferris can be reached on 571-272-3123. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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